WHAT IS CLAIMED IS:

Sub Amdt. A

1. A method for forming an integrated circuit, comprising:

forming a first dielectric layer disposed outwardly from a semiconductor substrate;

forming a first intermediate structure comprising:

a floating gate layer disposed outwardly from the first dielectric layer;

a second dielectric layer disposed outwardly from the floating gate layer; and

a first polysilicon layer disposed outwardly from the second dielectric layer;

removing regions of the first intermediate structure to form at least one gate stack;

forming at least one dielectric isolation region after the formation of the gate stacks, wherein the at least one dielectric isolation region is disposed between two gate stacks.

2. The method of Claim 1, wherein forming a dielectric isolation region comprises:

growing an isolation oxide layer outwardly from the gate stacks;

depositing an isolation dielectric layer outwardly from and between the gate stacks; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

3. The method of Claim 1, wherein forming a dielectric isolation region comprises:

growing approximately 200 Å of oxide outwardly from the gate stacks;

depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

4. The method of Claim 1, wherein the steps of forming at least one gate stack and forming an isolation dielectric region comprise:

removing at least a portion of the first intermediate structure and the substrate to form a plurality of trenches disposed adjacently to a plurality of moats in the substrate and at least one gate stack disposed outwardly from a moat;

depositing an isolation dielectric layer outwardly from the trenches in the substrate and outwardly from and between the gate stacks;

growing an isolation oxide layer outwardly from the gate stack; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

5. The method of Claim 1, further comprising:

forming a plurality of trenches disposed adjacent to a plurality of moats in the semiconductor substrate; and

forming trench dielectric regions outwardly from the trenches in the substrate.

6. The method of Claim 5, wherein forming a dielectric isolation region comprises:

depositing a field oxide layer within the trenches;

growing approximately 200 Å of oxide outwardly from the gate stacks;

depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks outwardly from the field oxide layer; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

7. The method of Claim 1, wherein the second dielectric layer comprises a layer of oxide having a thickness of approximately 70 Å.

8. The method of Claim 1, further comprising depositing a hemispherical grain poly layer outwardly from the floating gate layer.

9. The method of Claim 1, wherein the floating gate layer comprises a rough outer surface.

10. The method of Claim 1, further comprising forming a peripheral dielectric layer outwardly from a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the at least one gate stack.

11. The method of Claim 1, further comprising:

forming a second polysilicon layer disposed outwardly from the first polysilicon layer and the dielectric isolation layer;

masking a portion of the second polysilicon layer disposed outwardly from a floating gate array region of the substrate, the floating gate array region disposed inwardly from the at least one gate stack;

removing a portion of the second polysilicon layer and a portion of the first intermediate structure disposed outwardly from a peripheral region of the substrate, the peripheral region disposed adjacent to the floating gate array region of the substrate;

deglazing a portion of the first dielectric layer disposed outwardly from the peripheral region of the substrate;

forming a peripheral dielectric layer outwardly from the peripheral region of the substrate and the second polysilicon layer;

forming a third polysilicon layer outwardly from the peripheral dielectric layer;

forming a peripheral gate pattern outwardly from the peripheral dielectric layer, the peripheral gate pattern masking at least one region of the third polysilicon layer where a peripheral gate will be formed;

removing exposed regions of the third polysilicon layer leaving at least one peripheral gate disposed outwardly from the peripheral region of the substrate.

12. An integrated circuit, comprising:

a first dielectric layer disposed outwardly from a substrate;

a plurality of gate stacks, each gate stack comprising:

a floating gate body disposed outwardly from the first dielectric layer;

a second dielectric region disposed outwardly from the floating gate body; and

a first polysilicon layer disposed outwardly from the second dielectric region; and

a plurality of dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks.

13. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by growing the isolation oxide layer outwardly from the gate stacks; depositing the isolation dielectric layer outwardly from and between the gate stacks; and removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

14. The integrated circuit of Claim 12, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by:

growing approximately 200 Å of oxide outwardly from the gate stacks;

depositing approximately 0.5 micrometers of oxide outwardly from and between the gate stacks; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

15. The integrated circuit of Claim 12, wherein the substrate comprises at least one trench disposed between two gate stacks; and

at least one moat disposed adjacent to the at least one trench and inwardly from the at least one gate stack.

16. The integrated circuit of Claim 15, wherein each dielectric isolation region comprises:

an isolation oxide layer; and

an isolation dielectric layer;

the dielectric isolation region formed by:

growing a layer of oxide outwardly from the gate stacks;

depositing a dielectric outwardly from and between the gate stacks and outwardly from the trenches in the substrate; and

removing at least a portion of the isolation oxide layer and the isolation dielectric layer to expose at least an outer surface of the first polysilicon layer.

17. The integrated circuit of Claim 12, wherein each second dielectric region comprises a layer of oxide having a thickness of approximately 70 Å.

18. The integrated circuit of Claim 12, wherein each gate stack further comprises a hemispherical grain poly layer disposed outwardly from the floating gate body.

19. The integrated circuit of Claim 12, wherein each floating gate body comprises a rough outer surface.

20. The integrated circuit of Claim 12, further comprising:

a second polysilicon layer disposed outwardly from the first polysilicon layer and the dielectric isolation regions;

a peripheral dielectric layer disposed outwardly from the second polysilicon layer and a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the gate stacks;

at least one peripheral gate body disposed outwardly from the peripheral region of the substrate.